Title: **TRENCH ISOLATION STRUCTURE AND METHOD OF FORMING THE SAME**

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Field of Invention

[0001] The present invention generally relates to an isolation structure and a method of forming the same, and more particularly, to a trench isolation structure and a method of forming the trench isolation structure having a polysilicon liner.

Background of the Invention

[0002] Semiconductor devices typically include multiple individual components formed on or within a substrate. The way to prevent unwanted components or structures from cross talk or shorting becomes significantly important, since the integration circuit density is continuously increased. Therefore, isolation techniques are very critical for the purpose of electrically insulating various portions or structures of the semiconductor device from other portions of the device. A popular isolation technology used for sub-micron ultra-large scaled integrated (ULSI) technology is a technique known as "shallow trench isolation (STI)".

[0003] Conventional trench processes includes etching a substrate surface to a depth, and then refilling the trench with a deposited dielectric layer. The dielectric layer is then planarized to complete the trench isolation structure. However, as the feature size shrinks and the aspect ratio of the trench increases, the gap filling ability becomes an important factor in selecting the filled dielectric material. Comparing to conventional deposition processes, spin-on glass processes have the advantage of excellent gap filling ability in filling trenches. Therefore, the spin-on glass becomes one of selected dielectric materials

to fill the trench. Generally, the spin-on glass is formed by spin-coating a dielectric material over the substrate. Then, the coated dielectric material is annealed. The spin-on glass is then etched back to form a recess. A dielectric layer is subsequently deposited in the recess upon the spin-on glass. However, after the high temperature annealing process, the crack issue is likely to occur due to poor adhesion between the trench sidewall surfaces and the spin-on glass. The cracks between the spin-on glass and the trench sidewalls will reduce the isolation capability and a breakdown of the trench isolation may occur.

[0004] Therefore, there is a need to provide a trench isolation structure and a method of forming a trench isolation structure with enhanced adhesion between the filled dielectric layer and the trench sidewalls.

Summary of the Invention

[0005] One aspect of the present invention is to provide a method of forming a trench isolation structure which implements a polysilicon liner to enhance the adhesion between the spin-on glass and trench sidewalls.

[0006] Another aspect of the present invention is to provide a method of forming a trench isolation structure which implements an annealing step to convert a polysilicon liner into an oxide layer to prevent the crack issue when the trench is filled with the spin-on glass.

[0007] In one embodiment of the present invention, a method of forming a trench isolation structure includes providing a substrate having a trench etched therein. A polysilicon liner is formed in the trench. A dielectric layer, such as spin-on glass is formed in the trench upon the polysilicon liner.

[0008] The step of forming the dielectric layer includes coating a spin-on glass over the substrate. A chemical mechanical polishing is preformed on the spin-on glass, which is then annealed and etched back to form a recess. During the annealing step, the polysilicon

liner is converted into an oxide layer. The method further includes forming a filled dielectric layer, such as high density plasma formed oxide layer, in the recess upon the spin-on glass.

[0009] A further aspect of the present invention is to provide a trench isolation structure in a semiconductor substrate. The trench isolation structure includes a trench formed in the semiconductor substrate, a polysilicon liner arranged upon sidewall surfaces and a base surface of the trench, a spin-on glass arranged within the trench upon the polysilicon liner, and a filled dielectric layer arranged within the trench. The spin-on glass is interposed between the polysilicon liner and the filled dielectric layer. Moreover, the trench structure further includes an oxide layer converted from the polysilicon liner.

Brief Description of the Drawings

[0010] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0011] Figs. 1 to 6 illustrate cross-sectional views of forming a trench isolation structure in one embodiment of the present invention.

Detailed Description of the Invention

[0012] The present invention discloses a trench isolation structure and a method of forming the same, which implements a polysilicon liner to enhance the adhesion between trench sidewalls and spin-on glass to prevent the crack issue. Figures 1 to 6 illustrate preferred embodiments of the present invention.

[0013] Referring to Fig. 1, in one embodiment, a method of forming a trench isolation structure 10 is provided. The method includes providing a substrate 12 having a trench 14. The substrate 12 can be a semiconductor substrate, such as a silicon wafer, a silicon-containing substrate, or any substrate in need of isolation structure as appropriate. The trench 14 can be formed by conventional processes, such as lithography, etch, etc. As shown in Fig. 2, a polysilicon liner 16 is formed in the trench 14. The polysilicon liner 16 can be formed by conventional deposition processes and preferably has a thickness of about 50-150 angstroms.

[0014] Referring to Fig. 3, a dielectric layer 18 is formed in the trench 14 upon the polysilicon liner 16. The dielectric layer 18 includes a spin-on glass. For example, the step of forming the dielectric layer 18 includes coating a spin-on glass over the substrate 12. A baking step is performed after the spin-on glass is coated. As shown in Fig. 4, the dielectric layer 18 is planarized to expose the substrate 12. In other words, a chemical mechanical polishing is performed on the spin-on glass 18 to expose the substrate 12. An annealing step is performed so as to convert the polysilicon liner 16 into an oxide layer 22. It is noted that the polysilicon liner 16 can be converted into the oxide layer 22, so as to enhance the adhesion between the spin-on glass and the trench sidewalls and prevent the crack issue.

[0015] Referring to Fig. 5, the spin-on glass 18 is etched back to form a recess 20. For example, a wet etch process is performed on the spin-on glass 18 to create the recess 20 to a depth of about 500 to 1000 angstroms into the substrate 12. As shown in Fig. 6, a filled dielectric layer 24 is formed in the recess 20 upon the dielectric layer 18. The filled dielectric layer 24 can be formed by conventional processes, such as deposition, planarization, etc. For example, the filled dielectric layer 24 can be an oxide layer formed by high density plasma deposition processes, and then planarized by chemical mechanical

polishing processes. Therefore, the trench isolation structure 10 with excellent adhesion between the spin-on glass and trench sidewalls is formed by implementing the polysilicon liner 16.

[0016] In another embodiment, a trench isolation structure 10 in a semiconductor substrate 12 is provided. As shown in Fig. 6, the trench isolation structure 10 includes a trench 14 formed in the semiconductor substrate 12, a polysilicon liner 16 arranged upon sidewall surfaces and a base surface of the trench 14, a spin-on glass arranged within the trench 14 upon the polysilicon liner 16, and a filled dielectric layer 24 arranged within the trench 14. The spin-on glass 18 is interposed between the polysilicon liner 16 and the filled dielectric layer 24. Furthermore, the trench isolation structure 10 includes an oxide layer 22, which is converted from the polysilicon liner 16. The filled dielectric layer 24 includes an oxide layer formed by high density plasma deposition processes.

[0017] Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.